What is claimed is:

1. Apparatus comprising:

a main memory;

an information processor operatively coupled to said main memory and having (a) a normal-operation mode in which coherence control is performed for making data in a cache memory of a processor identical to data in a main memory and (b) a power-saving mode in which coherence control is suppressed to lower the power consumption from the power consumption of the processor when in said normal-operation mode, said processor entering said normal-operation mode when an input/output device accesses main memory while said processor is in said power-saving mode;

an attribute setting module for setting a device area of said main memory to a non-cacheable attribute for exempting said device area from coherence control even in said normal-operation mode, said device area being the area accessed by the input/output device of said information processor; and

an operation mode setting module for allowing said input/output device to access said device area while keeping the operation mode of said information processor in said power-saving mode when said input/output device requests access to said device area in said power-saving mode.

2. Apparatus according to claim 1, wherein if a device different from said input/output device accesses an area in said memory that is set to a cacheable attribute requiring said coherence control in said normal-operation mode, said operation mode setting module changes the operation mode of said information processor to the normal-operation mode.

3. Apparatus according to claim 1, wherein when said processor receives in said power-saving mode an access request signal provided from said input/output device to access said main memory, said processor changes the operation mode of said information processor to said normal-operation mode, and said operation mode setting module invalidates said access request signal to allow said input/output device to access said device area while keeping the operation mode of said information processor in said power-saving mode.

4. Apparatus according to claim 3, further comprising:

a register module for associating each of a plurality of pieces of mask data with each of a plurality of input/output devices and storing said mask data, said mask data specifying whether or not said access request signal received from each of said input/output device is invalidated;

a masking module for obtaining said access request signal for each input/output device and masking said access request signal with said mask data being associated with said input/output device and stored in said register module; and

an input module for inputting the input signal masked by said masking module into a processor to change the operation mode of said information processor;

wherein said operation mode setting module associates mask data invalidating said access request signal with said input/output device accessing said device area and stores said mask data in said register module to allow said input/output device to access said device area while keeping the operation mode of said information processor in said power-saving mode.

5. A program for causing a computer to function as an information processor having a normal-operation mode in which coherence control is performed for making data in a cache memory of a processor identical to data in a main memory and a power-saving mode in which said coherence control is suppressed to lower the power consumption from power consumption in said normal-operation mode and entering said normal-operation mode when an input/output device accesses said main memory in said power-saving mode, said computer being caused to function as:

an attribute setting module for setting a device area of said main memory to a non-cacheable attribute for exempting said device area from said coherence control even in said normal-operation mode, said device area being the area accessed by the input/output device of said information processor;

an operation mode setting module for allowing said input/output device to access said device area while keeping the operation mode of said information processor in said power-saving mode when said input/output device requests access to said device area in said power-saving mode.

6. The program according to claim 5, wherein when said processor receives in said power-saving mode an access request signal provided from said input/output device to access said main memory, said processor changes the operation mode of said information processor to said normal-operation mode; and said operation mode setting module invalidates said access request signal to allow said input/output device to access said device area while keeping the operation mode of said information processor in said power-saving mode.

7. A storage medium on which the program according to claim 5 or 6 is stored.

8. A control circuit for controlling mode selection in an information processor having a normal-operation mode in which coherence control is performed for making data in a cache memory identical to data in a main memory and a power-saving mode in which said coherence control is suppressed to lower the power consumption from power consumption in said normal-operation mode and entering said normal-operation mode when an input/output device accesses said main memory in said power-saving mode, comprising:

a register module for storing mask data for each input/output device, said mask data indicating whether or not an access request signal provided by each of a plurality of input/output devices for accessing said main memory is invalidated;

a masking module for obtaining said access request signal for each input/output device and masking said access request with mask data associated with said input/output device and stored in said register module; and

an input module for entering a signal masked by said masking module into a processor to switch the operation mode of said information processor.